CLAIMS

[0053] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming a recessed gate structure, comprising the acts of:

forming insulating columns over a semiconductor substrate;

using adjacent insulating columns as a guide to form a trench within said semiconductor substrate between said adjacent insulating columns;

forming a gate oxide on the bottom and sidewalls of said trench; and

forming a conductive region within and above said trench.

2. The method of claim 1, wherein said insulating columns are spaced apart from each other by a distance of about 50 nm to about 100 nm.

3. The method of claim 2, wherein said distance is about 80 nm.

4. The method of claim 1, wherein said insulating columns are formed to a height of about 20 nm to about 800 nm.

5. The method of claim 1, wherein said trench is etched to a depth of about 200 nm to about 700 nm.

6. The method of claim 2, wherein said trench is formed to a width of less than about 75% of said distance.

7. The method of claim 1, wherein said conductive region comprises polysilicon.

8. The method of claim 1, wherein said conductive region comprises a metal.

9. The method of claim 1, wherein said conductive region comprises a silicide.

10. The method of claim 9, wherein said silicide is formed of a material selected from the group consisting of CoSi, TiSi, MoSi and NiSi.

11. The method of claim 9, wherein said conductive region further comprises an insulating material over said silicide.

12. The method of claim 11, wherein said insulating material is a nitride material or an etch-stop insulating material.

13. A method of forming a recessed gate structure, comprising the acts of:

forming insulating columns over a semiconductor substrate;

using adjacent insulating columns as a guide to form a trench within said semiconductor substrate between said adjacent insulating columns;

forming a gate oxide on the bottom and sidewalls of said trench;

forming a conductive region within and above said trench; and

forming source and drain regions within said semiconductor substrate on sides of said conductive region within said trench.

14. The method of claim 13, wherein said insulating columns are spaced apart from each other by a distance of about 50 nm to about 100 nm.

15. The method of claim 14, wherein said distance is about 80 nm.

16. The method of claim 13, wherein said insulating columns are formed to a height of about 20 nm to about 800 nm.

17. The method of claim 13, wherein said trench is etched to a depth of about 200 nm to about 700 nm.

18. The method of claim 14, wherein said trench is formed to a width of less than about 75% of said distance.

19. The method of claim 14, wherein said conductive region comprises polysilicon or a metal.

20. The method of claim 14, wherein said conductive region comprises a metal silicide.

21. The method of claim 20, wherein said metal silicide is formed of a material selected from the group consisting of CoSi, TiSi, MoSi and NiSi.

22. The method of claim 20, wherein said conductive region further comprises an insulating material over said metal silicide.

23. The method of claim 22, wherein said insulating material is a nitride material or an etch-stop insulating material.

24. A method of forming self-aligned recessed gate structures for a semiconductor device, comprising the acts of:

providing an insulating layer over a semiconductor substrate;

patterning said insulating layer to form a plurality of insulating columns spaced apart from each other and to expose regions of said semiconductor substrate;

providing an oxide layer over said regions of said semiconductor substrate;

providing a dielectric material on sidewalls of each of said plurality of insulating columns and over portions of said oxide layer;

defining a first set of trenches of a first width in said semiconductor substrate and extending through said oxide layer;

defining a second set of trenches of a second width in said semiconductor substrate, said second width being greater than said first width;

forming a gate oxide within said second set of trenches; and

forming a conductive layer over said gate oxide and within said second set of trenches to form a recessed conductive gate.

25. The method of claim 24, wherein said plurality of insulating columns are spaced apart from each other by a distance of about 50 nm to about 100 nm.

26. The method of claim 25, wherein said distance is about 80 nm.

27. The method of claim 24, wherein said plurality of insulating columns are formed to a height of about 20 nm to about 800 nm.

28. The method of claim 24, wherein said oxide layer is formed to a thickness of about 3 nm to about 20 nm.

29. The method of claim 24, wherein said act of providing said dielectric material on sidewalls of each of said plurality of insulating columns further comprises forming a dielectric layer over said oxide layer and over said columns and removing portions of said dielectric layer to form said dielectric material.

30. The method of claim 24, wherein first set of trenches are formed to a width of about 50% of said distance.

31. The method of claim 24, wherein said act of defining said first set of trenches further comprises etching said oxide layer and said semiconductor substrate with a first etchant.

32. The method of claim 31, wherein said act of defining said first set of trenches further comprises removing said oxide layer and removing portions of said dielectric material to form a dielectric residue on said sidewalls of said insulating columns and adjacent said semiconductor substrate.

33. The method of claim 31, wherein said first ecthant has a selectivity to oxide in an HBr ambient.

34. The method of claim 31, wherein said first set of trenches are formed to a depth of about 100 nm to about 500 nm.

35. The method of claim 25, wherein said second set of trenches are formed to a width of about less than 75% of said distance.

36. The method of claim 24, wherein said act of defining said second set of trenches further comprises the act of etching said semiconductor substrate with a second etchant.

37. The method of claim 36, wherein said act of defining said second set of trenches further comprises removing said dielectric residue.

38. The method of claim 36, wherein said second etchant is a TMAH etchant.

39. The method of claim 36, wherein said second set of trenches are formed to a depth of about 200 nm to about 700 nm.

40. The method of claim 24, wherein said act of forming said conductive layer further comprises providing a polysilicon layer to completely fill said second set of trenches and to extend in between adjacent insulating columns by about 5 nm to about 100 nm.

41. The method of claim 24 further comprising the acts of:

forming a transition metal layer over said conductive layer and in between said adjacent insulating columns;

forming a cap layer over said transition metal layer and in between adjacent insulating columns;

removing said insulating columns; and

forming insulating spacers on sidewalls of said self-aligned recessed gate structures.

42. The method of claim 41, wherein said cap layer is formed of a nitride material.

43. The method of claim 41, wherein said cap layer is formed of an etch-stop insulating material.

44. A method of forming self-aligned recessed gate structures for a semiconductor device, comprising:

forming a plurality of isolation regions over a semiconductor substrate, said isolation regions comprising a dielectric material;

forming a first insulating layer over said semiconductor substrate;

patterning said first insulating layer to form a plurality of columns spaced apart from each other by a distance of about 50 nm to about 100 nm, and to form first exposed regions of said semiconductor substrate and second exposed regions of said dielectric material;

forming an oxide layer over said first exposed regions of said semiconductor substrate but not over said second exposed regions of said dielectric material;

forming a second insulating layer over said plurality of columns, and over said oxide layer and said dielectric material;

selectively etching said second insulating layer to form insulating spacers on sidewalls of each of said plurality of columns spaced apart from each other and over portions of said oxide layer and over said dielectric material;

defining a first set of trenches of a first width in said semiconductor substrate and extending through said oxide layer;

defining a plurality of recesses within said dielectric material of said plurality of isolation regions;

defining a second set of trenches of a second width in said semiconductor substrate, said second width being greater than said first width;

forming a gate oxide within said second set of trenches;

forming a conductive layer over said gate oxide, within said second set of trenches and within said plurality of recesses to form a first plurality of recessed conductive gates corresponding to said second set of trenches and a second plurality of recessed conductive gates corresponding to said plurality of recesses; and

providing a cap material over said first and second plurality of recessed conductive gates and extending in between said adjacent columns.

45. The method of claim 44, wherein said first set of trenches are etched to a depth of about 100 nm to about 500 nm.

46. The method of claim 44, wherein said first set of trenches are etched to a width of about 50% of said distance.

47. The method of claim 44, wherein said second set of trenches are etched to a depth of about 200 nm to about 700 nm.

48. The method of claim 44, wherein second set of trenches are formed to a width of less than about 75% of said distance.

49. The method of claim 44, wherein said plurality of recesses are etched within said dielectric material to a depth of about 1 nm to about 10 nm.

50. The method of claim 44, wherein said conductive layer is formed of polysilicon.

51. The method of claim 44, wherein said conductive layer is formed of a silicide.

52. The method of claim 51, wherein said silicide is formed of a material selected from the group consisting of CoSi, TiSi, MoSi and NiSi.

53. The method of claim 51, wherein said conductive layer further comprises an insulating material over said silicide.

54. The method of claim 53, wherein said insulating material is a nitride material or an etch-stop insulating material.

55. A method of forming a memory cell, comprising the acts of:

providing an insulating layer over a semiconductor substrate;

forming a transistor including a self-aligned recessed gate structure fabricated within said semiconductor substrate, a source and a drain region in said semiconductor substrate adjacent to said gate structure; and

forming a capacitor over said source/drain region, wherein said act of forming said transistor further comprises:

patterning said insulating layer to form a plurality of columns spaced apart from each other by a predetermined distance and to expose regions of said semiconductor substrate;

providing a sacrificial oxide layer over said regions of said semiconductor substrate;

providing a nitride material on sidewalls of each of said plurality of columns and over portions of said sacrificial oxide layer;

defining a first set of trenches of a first width in said semiconductor substrate and extending through said sacrificial oxide layer, said first width being about 50% of said predetermined distance;

removing portions of said nitride material and said sacrificial oxide layer to define a second set of trenches of a second width in said semiconductor substrate, said second width being greater than said first width but less than about 75% of said predetermined distance;

forming a gate oxide within said second set of trenches; and

forming a conductive layer over said gate oxide and within said second set of trenches to form said self-aligned recessed gate structure.

56. The method of claim 55, wherein said insulating layer is formed of a material selected from the group consisting of silicon nitride and silicon oxide.

57. The method of claim 55, wherein said memory cell is a DRAM memory cell.

58. The method of claim 55, wherein said memory cell is part of an integrated circuit.

59. The method of claim 55, wherein said memory cell is part of a memory circuit coupled to a processor.

60. The method of claim 59, wherein at least one of said processor and said memory circuit contains said self-aligned recessed gate structure.

61. The method of claim 55, wherein said conductive layer comprises a silicide.

62. The method of claim 61, wherein said silicide is a cobalt silicide, titanium silicide, molybdenum silicide or nickel silicide.

63. A self-aligned recessed gate structure, comprising:

a first recessed gate region having a first width located below a surface of a semiconductor substrate; and

a second gate region having a second width adjacent said first recessed gate region, said second gate region extending above said surface of said semiconductor substrate by about 20 nm to about 800 nm.

64. The self-aligned recessed gate structure of claim 63, wherein said second width is greater than said first width.

65. The self-aligned recessed gate structure of claim 63, wherein said second width is of about 50 nm to about 100 nm.

66. The self-aligned recessed gate structure of claim 65, wherein said second width is about 80 nm.

67. The self-aligned recessed gate structure of claim 65, wherein said first width is of about 35 nm to about 75 nm.

68. The self-aligned recessed gate structure of claim 63, wherein said first width is of about 60 nm.

69. The self-aligned recessed gate structure of claim 63, wherein said first recessed gate region has a height of about 100 nm to about 1,000 nm.

70. The self-aligned recessed gate structure of claim 63, wherein at least one of said first and second recessed gate regions comprises polysilicon material.

71. The self-aligned recessed gate structure of claim 63, wherein at least one of said first and second gate regions comprises a metal.

72. The self-aligned recessed gate structure of claim 63, wherein at least one of said first and second gate regions comprises a silicide.

73. The self-aligned recessed gate structure of claim 72, wherein said silicide is cobalt silicide, titanium silicide, molybdenum silicide or nickel silicide.

74. The self-aligned recessed gate structure of claim 72 further comprising an insulating layer over said silicide.

75. The self-aligned recessed gate structure of claim 74, wherein said insulating layer comprises a nitride material.

76. The self-aligned recessed gate structure of claim 74, wherein said insulating layer comprises an etch-stop insulating material.

77. The self-aligned recessed gate structure of claim 63 further comprising a transition metal layer over said second gate region.

78. The self-aligned recessed gate structure of claim 63 further comprising a nitride cap material over said transition metal layer.

79. A self-aligned recessed gate structure, comprising:

a first recessed gate region having a first width of about 35 nm to about 75 nm, said first recessed gate region being located below a surface of a semiconductor substrate;

a second gate region having a width of second about 50 nm to about 100 nm, said second gate region extending above said surface of said semiconductor substrate by about 20 nm to about 800 nm; and

insulating spacers located on sidewalls of said second gate region but not on sidewalls of said first recessed gate region.

80. The self-aligned recessed gate structure of claim 79, wherein said second width is about 80 nm.

81. The self-aligned recessed gate structure of claim 79, wherein said first width is about 60 nm.

82. The self-aligned recessed gate structure of claim 79, wherein said first and second recessed gate regions comprise a conductive material.

83. The self-aligned recessed gate structure of claim 82, wherein said conductive material is a silicide.

84. The self-aligned recessed gate structure of claim 83, wherein said silicide is formed of a material selected from the group consisting of CoSi, TiSi, MoSi and NiSi.

85. The self-aligned recessed gate structure of claim 79, wherein said first and second recessed gate regions comprise polysilicon material.

86. The self-aligned recessed gate structure of claim 79 further comprising a transition metal layer over said second gate region.

87. The self-aligned recessed gate structure of claim 79 further comprising a nitride cap material over said transition metal layer.

88. A memory cell, comprising:

a silicon substrate;

a transistor including a self-aligned recessed gate structure fabricated within said silicon substrate, wherein said self-aligned recessed gate structure further comprises a first recessed gate region having a first width located below a surface of said silicon substrate; a second gate region having a second width greater than said first width, said second gate region extending above said surface of said semiconductor substrate;

a doped region in said silicon substrate disposed adjacent to said gate structure; and

a capacitor formed over and electrically connected with said doped region.

89. The memory cell of claim 88, wherein said second gate region extends above said surface of said semiconductor substrate by about 20 nm to about 800 nm.

90. The memory cell of claim 89, wherein said second gate region extends above said surface of said semiconductor substrate by about 200 nm.

91. The memory cell of claim 88, wherein said second width is about 25% greater than said first width.

92. The memory cell of claim 88, wherein said first and second recessed gate regions comprise a conductive material.

93. The memory cell of claim 92, wherein said conductive material is a silicide.

94. The memory cell of claim 93, wherein said silicide is formed of a material selected from the group consisting of CoSi, TiSi, MoSi and NiSi.

95. The memory cell of claim 93 further comprising a cap material over said silicide.

96. The memory cell of claim 95, wherein said cap material is formed of a nitride material or an etch-stop insulating material.

97. The memory cell of claim 88, wherein said memory cell is a DRAM memory cell.

98. The memory cell of claim 88, wherein said memory cell is part of a memory circuit coupled to a processor.

99. The memory cell of claim 98, wherein at least one of said processor and said memory circuit contains said gate structure.